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12EC025

M.Tech. Degree Examination, Dec.2014/Jan.2015
Design of Analog and Mixed Mode VLSI Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Derive and explain I/V characteristics of MOSFET. **(12 Marks)**

b. Explain the following second order effects of MOSFET: i) Body effect; ii) Channel length modulation. **(08 Marks)**

2 a. Explain common-source stage with resistive load and draw small signal model of common source stage including the transistor o/p resistance. **(10 Marks)**

b. Explain source follower with its input-output characteristics and also draw small signal equivalent circuit of source follower. **(10 Marks)**

3 a. Explain miller effect using Miller's theorem. **(06 Marks)**

b. Draw and explain high frequency model of a cascade stage. **(08 Marks)**

c. Neglecting channel-length modulation, compute the transfer function of the common-gate stage shown in Fig.Q.3(c). **(06 Marks)**

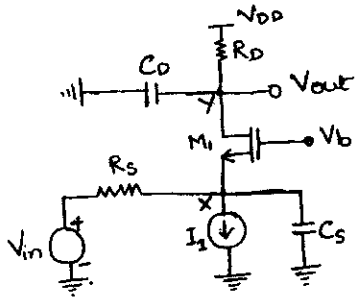

Fig.Q.3(c)

4 a. Explain differential pair with MOS loads and explain how voltage gain increased for the same. **(08 Marks)**

b. Explain cascade current mirrors. **(12 Marks)**

5 a. In the circuit of Fig.Q.5(a), assume the Op-Amp is a single-pole voltage amplifier. If V_{in} is a small step calculate the time required for the o/p voltage to reach within 1% of its final value. What unity-gain bandwidth must the op-amp provide if $1+ R_1/R_2 \approx 10$ and the settling time is to be less than 5ns? For simplicity, assume the low-frequency gain is much greater than unity. **(10 Marks)**

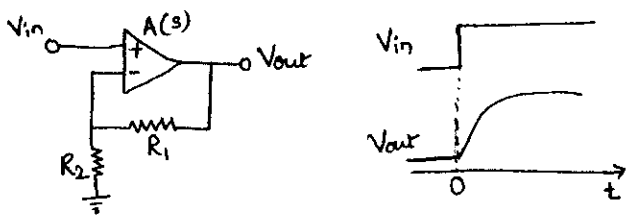

Fig.Q.5(a)

b. Explain folded cascade op-amp with cascade PMOS loads and determine the small signal voltage gain. **(10 Marks)**

6 a. Write a note on the performance parameters of voltage controlled oscillator. **(10 Marks)**
b. What is PLL? Explain basic PLL topology with neat diagrams. **(10 Marks)**

7 a. Explain the following: i) Negative TC voltage ; ii) Positive TC voltage. **(10 Marks)**
b. Explain switched capacitor integrator with neat diagrams. **(10 Marks)**

8 a. Explain DAC specification with figures. **(10 Marks)**
b. Explain flash ADC architecture with the help of block diagram and principle of conversion with an example for 3 bits. **(10 Marks)**

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